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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,364	12/19/2001	Kuang-Yeh Chang	NAUP0409USA	3924
27765	7765 7590 03/08/2005		EXAMINER	
NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC) P.O. BOX 506 MERRIFIELD, VA 22116			WARREN, MATTHEW E	
			ART UNIT	PAPER NUMBER
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			DATE MAILED: 03/08/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

1
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Office Action Summary Saminer		Application No.	Applicant(s)				
Mathew E. Warten ### Warten		09/683,364	CHANG ET AL.				
The MALING DATE of this communication appears on the cover sheet with the correspondence address → Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. Eletrecises for the may be available used the previsions of 12 CR 1.13(a), in no event, however, may a reply be timely filled in the period for reply a specified above. See that the third (30) says, an pay within the statisticy minimum of thirty (30) days will be considered timely. If the period for reply a specified shows the transfer that the period for reply a specified shows the transfer that they show the transfer and value gains (31) (MONTHS from the mailing date of this communication. Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any search galactic than displaced the mailing date of this communication, even if timely filed, may reduce any search galactic than a displaced to the communication, even if timely filed, may reduce any search galactic than the process of the communication, even if timely filed, may reduce any search galactic than the file of the communication, even if timely filed, may reduce any search galactic than the process of the communication of the mailing date of this communication, even if timely filed, may reduce any search galactic than the process of the mailing date of this communication. Status 1) □ Responsive to communication (s) filed on 20 December 2004. 20 □ Claim (s) □ Since this application is no condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Expanded Transfer (and the process of the merits is closed in a coordance with the practice under Expanded Transfer (and the process of the merits is closed in a coordance and the process of the process	Office Action Summary	Examiner	Art Unit				
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DETAILED ACTION

This Office Action is in response to the RCE and Amendment filed on December 20, 2004.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20, 21, and 23-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's prior art figure (APAF) in view of Yamazaki et al. (US 6,677,613 B1).

In re claims 20 and 29, the APAF 1 and 7 shows a microdisplay pixel cell device, the device comprising a semiconductor substrate defined with a plurality of active areas or a plurality of transistors; two gates (12 in fig. 1 or 52 in fig. 7), the gates covering a portion of the active area, four sources (b) and two drains (a) (or 63/64 in fig. 7), the source/drain being in the active area, and a first dielectric layer (66 in fig. 7) the first dielectric layer covering the gate and the source/drain. The first dielectric layer comprises at least one row select contact plug (68) to electrically connect to one of the gates and at least one row select line, the row select line being atop the first dielectric layer, the row select line being electrically connected to the gate through the row select contact plug. There are four pixel cap top plates (20 in fig. 1 or 42 in fig. 7) on the first

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dielectric layer (or a plurality of pixel cap top plates), at least one capacitor dielectric layer (45), the capacitor dielectric layer being atop the surface of the top plate; and at least one pixel cap bottom plate (22). At least one first contact plug is comprised in the first dielectric layer for electrically connecting the source and the top plate (APAF 1, and pg. 2, para. [0007]). The APAF 7 shows all of the elements of the claims except the second dielectric layer being atop the first dielectric layer and the pixel cap top plates partially covering one of the active areas and the gates. Yamazaki et al. shows (figs. 1A-3) a pixel cell device comprising a first dielectric layer (125) formed over a gate (109), and a second dielectric layer (134) formed on the first dielectric layer. Yamazaki also shows a pixel cap bottom plate (139) being atop the second dielectric layer and covering a capacitor top plate (135) and a capacitor dielectric layer (135). The pixel cap top plate covers one of the active areas and the gates. With the capacitor being formed simultaneously with the light shielding layer, the area of the pixel electrode could be reduced and a sufficient capacitance could be provided (col. 9, lines 29-35). Therefore it would have been obvious to one of ordinary skill in the art a the time the invention was made to modify the pixel device of the APAF by adding a second dielectric layer and forming the four pixel cap plates over the active areas and gate as taught by Yamazaki so that the capacitor top plates can simultaneously be formed with a light shielding layer to ultimately reduce a pixel area and form a sufficient capacitor.

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In re claim 21, the APAF 7 shows that the gate comprises a gate oxide layer (44), a polysilicon layer or a metal silicide layer.

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In re claims 23 and 31, the APAF 1 discloses (pg. 2, para. [0007]) that at least one second contact plug (145) is comprised in the first dielectric layer and the second dielectric layer for electrically connecting the drain to a video data line.

In re claims 24 and 32, the APAF 7 discloses (pg. 4, para. [0014]) that the row select line is composed of a metal and is used as a scan line of the microdisplay.

In re claims 25 and 33, the APAF 7 discloses (pg. 4, parà [0016]) that both the bottom plate and the top plate are composed of a metal.

In re claims 26 and 34, Yamazaki et al. discloses (col. 6, lines 43-52 and col. 9, lines 1-7) that both the bottom plate and the top plate are composed of titanium (Ti), titanium nitride (TiN), aluminum (Al), copper (Cu) or an alloy of above-mentioned materials.

In re claims 27 and 35, the APAF 1 discloses (pg. 2, para. [0007]) the pixel cell comprises two gates (12), two common drains (a), four sources (b), four top plates (20) and one bottom plate (22). The APAF 7 shows that the items are stacked in a sequence from bottom to top.

In re claims 28 and 37, the APAF 7 discloses (pg. 2, para. [0006]) that the microdisplay is a reflective liquid crystal on silicon (LCOS) display.

In re claim 30, the APAF 7 shows at least one first contact plug is comprised in the first dielectric layer for electrically connecting the source and the top plate (APAF 1, and pg. 2, para. [0007]). When combined with Yamazaki, the contact plug is comprised in the first and second dielectric layer for connecting the source and one of the top plates.

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In re claim 36, the APAF 1 shows that the microdisplay pixel device comprises four top plates (20). When combined with Yamazaki, the four top plates of the APAF would cover the four transistors in the block just as Yamazaki's top plate covers the transistor in fig. 3.

Response to Arguments

Applicant's arguments filed with respect to claims 20-37 have been fully considered but they are not persuasive. The applicant primarily asserts that the prior art references do not show all of the limitations of the amended claims, specifically that the references do not show four pixel cap top plates (or plurality of cap top plates) and one pixel cap bottom plate being disposed atop the transistor block. As stated in the rejection above, the APAF showed all of the elements of the claims except the second dielectric layer and the pixel cap bottom plates formed atop the transistor block. The APAF 1 shows a side view in which there are four cap top plates (20) (or a plurality of cap top plates) and two cap bottom plates (22) (which is at least one cap bottom plate). The only major limitation not shown in the APAF 1 is the four pixel cap top plates (or plurality of cap top plates) partially cover one of the active areas and one of the gates. The cap plates of the APAF are formed to the side of the active area. Yamazaki cured the deficiencies of the APAF by showing that the cap plates are formed over the active area and the gate to simultaneously form a light shielding layer and reduce the area of the pixel electrode.

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The limitation of "at least one pixel cap bottom plate" is interpreted to mean that there is one or more cap bottom plates. The APAF 1 shows that there are two cap bottom plates (22), each one covering a plurality (two) of cap top plates (20). Because the limitations concerning the at least one pixel cap bottom plate are broadly written, the prior art references disclose all of the limitations of the claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW MEW

March 3, 2004

TOM THOMAS

SUPERVISORY PATENT EXAMENER